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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,065	02/20/2004	Takeshi Shimizu	073338.0177 (04-50094 FLA	6302
5073 BAKER BOTT	7590 07/27/2007 'S L.L.P.	EXAMINER		
2001 ROSS AVENUE SUITE 600 DALLAS, TX 75201-2980			JONES, PRENELL P	
			ART UNIT	PAPER NUMBER
			2616	
		•	NOTIFICATION DATE	DELIVERY MODE
			07/27/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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•	Application No.	Applicant(s)			
Office Asking Comment	10/783,065	SHIMIZU ET AL.			
Office Action Summary	Examiner	Art Unit			
	Prenell P. Jones	2616			
The MAILING DATE of this communication Period for Reply	appears on the cover sheet wi	th the correspondence address			
A SHORTENED STATUTORY PERIOD FOR RE WHICHEVER IS LONGER, FROM THE MAILING - Extensions of time may be available under the provisions of 37 CFR after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period for reply within the set or extended period for reply will, by standard part of the mailing after the matter than three months after the meanned patent term adjustment. See 37 CFR 1.704(b).	B DATE OF THIS COMMUNIC R 1.136(a). In no event, however, may a narricological control of the co	CATION. eply be timely filed ITHS from the mailing date of this communication. BANDONED (35 U.S.C. \$ 133)			
Status		·			
1) Responsive to communication(s) filed on 11	2 December 2005.				
2a) ☐ This action is FINAL . 2b) ☑ 1					
3) Since this application is in condition for allo	wance except for formal matt	ers, prosecution as to the merits is			
closed in accordance with the practice unde	er <i>Ex parte Quayle</i> , 1935 C.D	. 11, 453 O.G. 213.			
Disposition of Claims					
4)⊠ Claim(s) <u>1-22</u> is/are pending in the applicat	ion.				
4a) Of the above claim(s) is/are without					
5) Claim(s) is/are allowed.					
6) ⊠ Claim(s) <u>1-22</u> is/are rejected.					
7) Claim(s) is/are objected to.					
8) Claim(s) are subject to restriction an	d/or election requirement.				
Application Papers					
9) The specification is objected to by the Exam	niner.				
10) The drawing(s) filed on is/are: a) a	accepted or b) objected to	by the Examiner.			
Applicant may not request that any objection to	the drawing(s) be held in abeyan	nce. See 37 CFR 1.85(a).			
Replacement drawing sheet(s) including the cor					
11)☐ The oath or declaration is objected to by the	Examiner. Note the attached	d Office Action or form PTO-152.			
Priority under 35 U.S.C. § 119					
12) Acknowledgment is made of a claim for fore a) All b) Some * c) None of:	•	3 119(a)-(d) or (f).			
1. Certified copies of the priority docum					
2. Certified copies of the priority docum		·· ——			
3. Copies of the certified copies of the p	•	received in this National Stage			
application from the International Bur * See the attached detailed Office action for a		received			
dec the attached detailed office action for a	nst of the certified copies not	received.			
Attachment(s)	_				
 Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTO-948) 		Summary (PTO-413) s)/Mail Date			
Notice of Drattsperson's Patent Drawing Review (P10-946) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date		nformal Patent Application			

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Claim Objections

- 1. Claims 1-18 are objected to because of the following informalities:
- 2. The term "operable" and "capable" in claims 1-18 makes the limitations following it to be optional, which renders the meads and bounds of the claim to be indefinite. Appropriate correction is required.

Claim Rejections - 35 USC § 103

- 3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).
- 4. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bellenger (US Pat 5,949,786) in view of Simmons et al (US Pat 6,084,856).

Regarding claim 1, 3, and 8, Bellenger discloses a communication a multi-protocol switch that manages and monitoring accessible locations for storing routing information, wherein the architecture includes multiple ports, tagging storage locations (Fig. 2, Abstract, col. 2, line 41-67, col. 4, line 47-56), a switch fabric for receiving packets between ports (Fig. 2, col. 4), multiple memory banks logically divided into a plurality of rows that include rows and storage

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units (Fig. 2, RDRAM), and a memory control module for receiving an memory access request from ports, and determining rows bas on address indicated by the request (Figs. 2-5, col, 5).

However, Bellenger is silent on overflow buffer having multiple storage location and maintaining routing entry and to access row and the overflow buffer to perform a memory access operation.

In a switch communication system, Simmons discloses managing and monitoring storing data in registers/storage locations, whereby network traffic is stored, which include MIB counter values (management information base), and configured registers in a switch are based on rate rate-based network traffic derived from MIB counter values, and overflow buffers along with (Fig. 4, 5 & 7A, Abstract), memory in switch providing overflow regions with respect to network ports (col. 2, line 41-56), wherein buffer manager uses control queues for buffer pool (col. 8, line 29-59), and overflow areas store excess entries that fail to fit in control queues (col. 10, line 8-65), and overflow buffer transfers data over data bus to memory in a DMA (direct access memory) transaction (col. 7, line 7, line 30 thru col. 8, line 28).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement overflow buffer having multiple storage location and maintaining routing entry and to access row and the overflow buffer to perform a memory access operation as taught by Simmons with the teachings of Bellenger for the purpose of further managing the storing of data flow in a switch environment whereas to minimize cost and increase efficiency.

Regarding 2, Bellenger further discloses address memory access requesting lookup operation (Fig. 2), and receiving routing entries from rows (col. 4, line 47 thru col. 5, line 61),

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each entry in route table contains tag (potential routing entries), accessed entries is used to determine a match (Fig. 3 & 6, col. 5, line 5-60)

Although, Bellenger is silent on overflow buffer and comparing address against each of the entries.

Simmons further discloses in a switch utilizing overflow management and monitoring with respect with overflow regions, wherein each port stores output of corresponding/matching port as associated with routing data, and decrease in size of base address (col. 13, line 5-46).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement overflow buffer including a matching entry, returning routing information from the matching entry, the routing information identifying at least one port, a switch utilizing overflow management and monitoring with respect with overflow regions, wherein each port stores output of corresponding/matching port as associated with routing data, and decrease in size of base address as taught by Simmons with the teachings of Bellenger for the purpose of further managing the storing of data flow in a switch environment whereas to minimize cost and increase efficiency.

Regarding claim 4, Bellenger further discloses an arbitration module to receive lookup/learn request (Fig. 2), and memory access module for a series of memory access operations (series of hash codes) to determine a hash key from an address indicates a specific row (col. 4, line 57-67, col. 6, line 34-60) generates and processes as associated with ports and generating hash keys wherein a row associated with a flow buffer is indicated by a hash key (col. 4, line 47-67).

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Regarding claim 5, Bellenger further discloses an arbitration module that schedules memory access operations with respect to lookup and learn request (Fig. 5, col. 6, line 21-60, col. 8, line 23-36, col. 9, line 7-46).

Regarding claim 6, Bellenger further an arbitration module servicing a learn request (Fig. 2, Fig. 5, col. 6, line 21-60, col. 8, line 23-36, col. 9, line 7-46) and determining whether a read operation detected a miss in a memory bank, whereas a write operation indicates a source to port map from learn request (Fig. 4, Abstract, col. 5, line 5-61).

Regarding claim 7, 12, 16 and 20, Bellenger further discloses flow detect filters, which stores data in registers, wherein the filters are used to select or de-select processing operations, such as write operation with respect to accessing memory (Abstract, col. 3, line 33-56).

Regarding claim 9, Bellenger further discloses storage elements associated with a plurality of ports and associated rows and flow buffers/overflow buffer for processing memory access (col. 4, line 23 thru col. 5, line 16, col. 6, line 21-34).

Regarding claim 10 and 15, as indicated above, combined Bellenger and Simmons discloses a communication a multi-protocol switch that manages and monitoring accessible locations for storing routing information, wherein the architecture includes multiple ports, tagging storage locations, a switch fabric for receiving packets between ports, multiple memory banks logically divided into a plurality of rows that include rows and storage units (Fig. 2, RDRAM), and a memory control module for receiving an memory access request from ports, and

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determining rows bas on address indicated by the request managing and monitoring storing data in registers/storage locations, whereby network traffic is stored, which include MIB counter values and configured registers in a switch are based on rate rate-based network traffic derived from MIB counter values, and overflow buffers along with, memory in switch providing overflow regions with respect to network ports, wherein buffer manager uses control queues for buffer pool, and overflow areas store excess entries that fail to fit in control queues, and overflow buffer transfers data over data bus to memory in a DMA transaction. Bellenger further discloses generating hash from flow, and determining hash key based on destination address, wherein matching of hash key and hash codes with respect to table for the addressed entries (Fig. 2, 5 & 6, col. 8, line 23-55)

Although, Bellenger is silent on overflow buffer including a matching entry, returning routing information from the matching entry, the routing information identifying at least one port, Simmons further discloses in a switch utilizing overflow management and monitoring with respect with overflow regions, wherein each port stores output of corresponding/matching port as associated with routing data, and decrease in size of base address (col. 13, line 5-46).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement overflow buffer including a matching entry, returning routing information from the matching entry, the routing information identifying at least one port, a switch utilizing overflow management and monitoring with respect with overflow regions, wherein each port stores output of corresponding/matching port as associated with routing data, and decrease in size of base address as taught by Simmons with the teachings of Bellenger for the purpose of further managing the storing of data flow in a switch environment whereas to minimize cost and increase efficiency.

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Claim 18 includes the limitations of method claim 10, but in the form of a physical switch. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement a switching architecture that is constructed to further implement the functions of claim 10.

Regarding claim 11 and 19, Bellenger further discloses learn/look-up processing wherein a routing table is associated with selected hash values and hash coding, wherein hash values are generated based on incoming address, and wherein the hash is utilized in conjunction with address and rows (Fig. 6, col. 3, line 33-55, col.4, line 50-67).

Regarding claims 13 and 14, Bellenger further discloses decision steps on matching address entries with respect to source and destination addresses (Figs. 3 & 4, col. 5, line 5-62), wherein rows of data are compared with "matching entries, as well as, determining addressable locations (available storage location) for storage (col. 2, line 51 thru col. 3, line 31, col. 4, line 47-67).

Claims 21 and 22 include the limitations encompassed in claims 13 and 14, but in the form of a switching device. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement a switching architecture that is constructed to further implement the functions claim 10.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prenell P. Jones whose telephone number is 571-272-3180. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on 571-272-3179. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Prenell P. Jones,

July 20, 2007)

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SUPERVISORY PATENT EXAMINED